Realization of Tuneable MOS-C Quadrature Sinusoidal Oscillator Using Composite Current Conveyor

Hasan Çiçekli, Ahmet Gökçen

Abstract—In this paper, a new voltage-mode MOS-C quadrature sinusoidal oscillator circuit based on composite second-generation current conveyor (CCCII) is presented. The proposed topology employs two CMOS based CCCII and four grounded components. CCCII is implemented by two CCII, so it also is possible to employ the circuit by commercially available AD844 by Analog Devices. The validity of the proposed circuit has been verified by PSPICE simulation programme. Simulation is done for both CMOS based implementation and AD844 based implementation of CCCII. It is seen that the simulation results agree well with the theoretical analysis and the proposed circuit achieves a good THD performance. The resistors used in the circuit are implemented by MOS transistors. So, the proposed circuit is fully integrable and it is possible to adjust the oscillation frequency by external MOS gate voltage. Also, it is stated how the CCCII employing circuit enhance the circuit performance when compared to the same topology employing CCII.

Keywords—Analog integrated circuits, Current conveyors, MOS-C realization, Oscillators.

I. INTRODUCTION

Quadrature sinusoidal oscillators find wide range of applications in telecommunication, signal processing, instrumentation, measurement and control systems and they can offer sinusoidal signals with 90° phase difference that is a requirement for some devices such as quadrature mixers, phase modulators and single-sideband generators [1]-[4]. For measurement purposes, quadrature sinusoidal oscillators are used as vector generators or selective voltmeters [5].

During recent years, several implementations of quadrature sinusoidal oscillators employing different high-performance active building blocks such as current feedback operational amplifier(CFOA), different types of current conveyor, four terminal floating nullor (FTFN), current follower, current differencing buffered amplifier (CDBA), current differencing transconductance amplifier (CDTA) and operational transresistance amplifier (OTRA) have been reported [6]-[21]. However, there is one or more drawbacks of these reported circuits such as excessive use of the passive elements, especially the external resistors, use of multiple-output active elements that makes the circuits more complicated, use of floating capacitor, which is not convenient for integration and the lack of electronic adjustment of the oscillation frequency.

The aim of this work is to present a new CCCII based quadrature sinusoidal oscillator realization and to do performance comparison to see how the CCCII based circuits have enhanced performance when compared to the same topology employing CCII. The features of the proposed circuit are as follows:

a) The capacitors and resistors used in the circuit are all grounded.
b) Resistors are implemented by MOS transistors, so the circuit is suitable for integration.
c) Electronic adjustment of the oscillation frequency.
d) Providing good characteristic with lower distortion than the oscillator circuit employing CCII.
e) Using only two active elements with single outputs.
f) Possibility to adjust the oscillation frequency without affecting the oscillation condition.
g) Possibility to employ the circuit by using commercially available AD844.

In the literature we have found, among the voltage mode quadrature sinusoidal oscillator circuits, none of them employs CCCII and have the whole features shown above.

II. CIRCUIT DESCRIPTION OF CCCII

The current conveyor is still emerging as one of the most important current-mode active building block and different types of current conveyor enable the researchers to design multipurpose circuits to be used in analog signal processing. CCCII can be constructed of two second generation current conveyors as shown in Fig.1 [22]. It is a useful technique to enhance the performance of the current conveyor by either lowering the x-terminal impedance or enhancing the y-terminal admittance [22]. This provides the CCCII based circuits have better output characteristics when compared to the same circuit topology employing CCII. In the CCCII-configuration, the lower conveyor CC2 works as a negative impedance conveyor and consequently the X-terminal impedance of the CCCII- is

$$Z_{x(composite)} = Z_{x1} + A_{i2}Z_{x2} \cong Z_{x1} - Z_{x2} \qquad (1)$$

It is clearly seen from (1) that the current gain A_{i2} should be designed slightly lower than the first in order to prevent a negative X-terminal impedance for the composite conveyor.

In addition, all even order nonlinearities in Z_{x1} and Z_{x2} are effectively summed together and hence X-terminal impedance nonlinearity is increased. Fortunately, in most cases the nonlinearity of the X-terminal impedance has little effect on the total amplifier distortion [22].

It is possible to implement the CCCII by using the current conveyor blocks as subcircuit. This current conveyor based CCCII implementation method makes it possible to employ the circuit by using commercially available AD844.
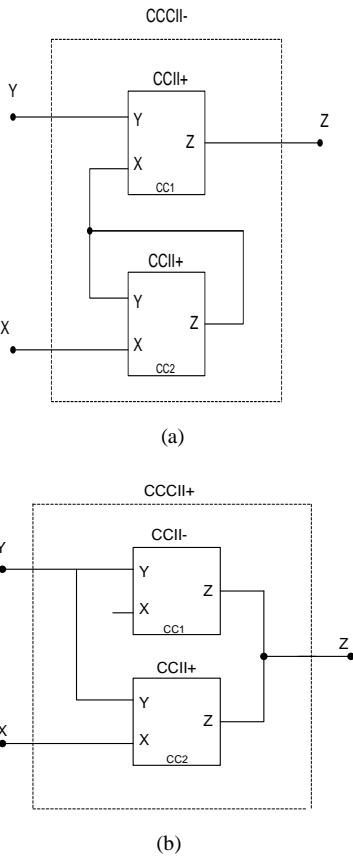
$$S_{R_1}^{\omega 0} = S_{R_2}^{\omega 0} = S_{C_1}^{\omega 0} = S_{C_2}^{\omega 0} = -1/2 \qquad (4)$$

As it is shown in (4), the sensitivities of passive components are quite low.

IV. MOS-C REALIZATION OF THE PROPOSED CIRCUIT

A linear resistor has been realized by using parallel connection of two depletion type NMOS transistors operated in the triode region as illustrated in Fig. 3 [23]. This method cancels out the non-linearity of the MOSFET significantly.
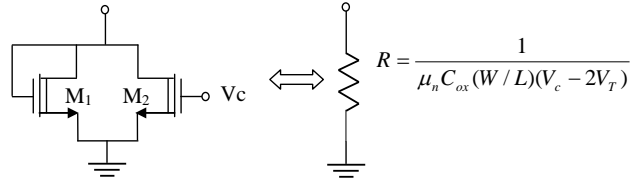
Fig. 3 Linear resistor realization using nonlinearity cancellation technique in parallel connection of two NMOS transistors

Where W and L are the channel width and length and V_T is the threshold voltage of the MOSFET, μ_n is the free electron mobility in the channel and C_{ox} is the gate oxide capacitance per unit area. The resistance values are tunable via V_C and since the even-order nonlinearities are cancelled out, it operates linearly over an extended voltage range. For achieving the fully MOS-C realization of the proposed oscillator circuit, the resistors must change with their MOS transistor conjugates.

Fig. 4 shows MOS-C realization of the proposed circuit. It is clear from this figure that the oscillation frequency of the circuit can be controlled by gate voltages V_{C1} and V_{C2} of the MOS transistors.
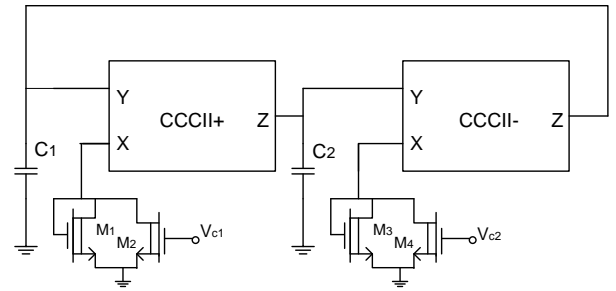
Fig. 4 MOS-C realization of the proposed circuit

V. SIMULATION RESULTS

The proposed circuit's performance has been evaluated for two different implementation of CCCII by PSPICE simulation programme using the MOSIS 0.35 μm CMOS process parameters and AD844 Macro-model parameters.

A. CMOS Based CCCII Simulation Results

The circuit schematic of CMOS CCII used to implement the CCCII is shown in Fig. 5 [24]. The circuit is supplied with symmetrical voltages of ±1.25 V. W/L parameters of MOS transistors used in simulation are as in [24].

The biasing currents are taken as $I_{B(CCII+)} = I_{B(CCII-)} = 5\ \mu A$. The passive component values taken in simulation

---

Fig. 1 Composite second-generation current conveyor implementation using CCIIs.
 (a) Composite CCII- with lower Zx.
 (b) Composite CCII+ with enhanced Yx.

III. PROPOSED CIRCUIT TOPOLOGY

The proposed CCCII based voltage-mode quadrature sinusoidal oscillator topology is shown in Fig. 2.
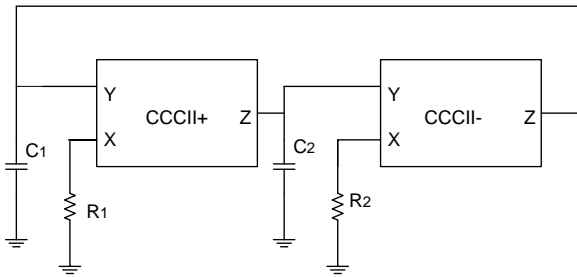

Fig. 2 Proposed circuit topology

The circuit analysis of the proposed quadrature sinusoidal oscillator yields the following characteristic equation

$$s^2 C_1 C_2 + G_1 G_2 = 0 \qquad (2)$$

The radian frequency of oscillation is

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \qquad (3)$$

The sensitivity of radian frequency to the passive components are all calculated as

are given in Table I. In the simulations, the process parameters of MOS transistors used to realize the resistors in Fig. 4, are taken as W=8.3 μm and L=0.7μm for all M1, M2, M3 and M4. MOS gate voltages are taken as $V_{C1}= V_{C2}$ =2.9 V and the resistor value is found as $R \cong 254$ Ω.
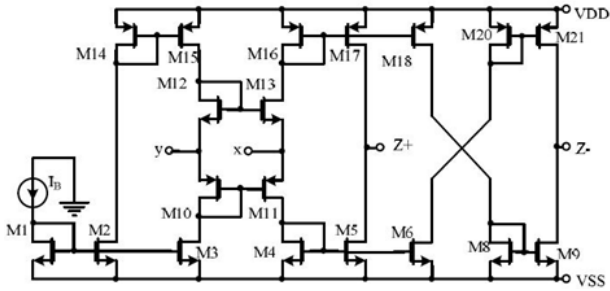

Fig. 5 Circuit schematic of dual output CMOS CCII used for CCCII implementation

TABLE I. PASSIVE COMPONENT VALUES

R_1	R_2	C_1	C_2
250 Ω	250 Ω	500 pF	500 pF

The calculated value of oscillation frequency is f_0= 1.27 MHz. In order to make a performance comparison, two simulations are done for the circuits employing CCII and CCCII. The oscillation frequency and total harmonic distortion (THD) values obtained from the simulations are given in Table II. V(1) and V(2) denote the voltages across the capacitors C_1 and C_2.

TABLE II. OSCILLATION FREQUENCY AND THD VALUES FOR CMOS IMPLEMENTATION

	Circuit employing CCII		Circuit employing CCCII	
Oscillation Frequency (MHz)	1.15		1.22	
THD %	V(1)	V(2)	V(1)	V(2)
	6.1	8.5	3.1	3.9

As it is seen from Table II, simulation results agree well with the theoretical calculations and the proposed circuit achieves a good THD performance. Table II also shows that the THD values of the circuit employing CCCII are significantly better than the values of the circuit employing CCII. The power dissipation of the circuit employing CCCII is 2.69 mW for the initial voltage of 0.2 mV given to C_1. The quadrature phase error is 1.98 % and the oscillation frequency deviation error is 3.93 % for the circuit employing CCCII.

In order to evaluate the tuneability of oscillation frequency, the gate voltages of M2 and M4, which are shown as V_{C1} and V_{C2}, are varied in a range of 2-3 V. The frequency values obtained by the variations of V_{C1} and V_{C2} are summarized in Table III.

TABLE III. THE OSCILLATION FREQUENCY AND THD VALUES OBTAINED BY THE VARIATION OF V_{C1} AND V_{C2}

V_{C1}, V_{C2} (V)	Oscillation Frequency (MHz)	THD %	
		V(1)	V(2)
2.0	0.87	1.0	1.7
2.2	0.96	1.6	2.5
2.4	1.04	0.9	1.3
2.6	1.10	1.0	0.8
2.8	1.19	2.1	2.4
3.0	1.26	5.4	3.7

The voltage waveforms of the proposed circuit employing CMOS based CCCII are shown in Fig.6.
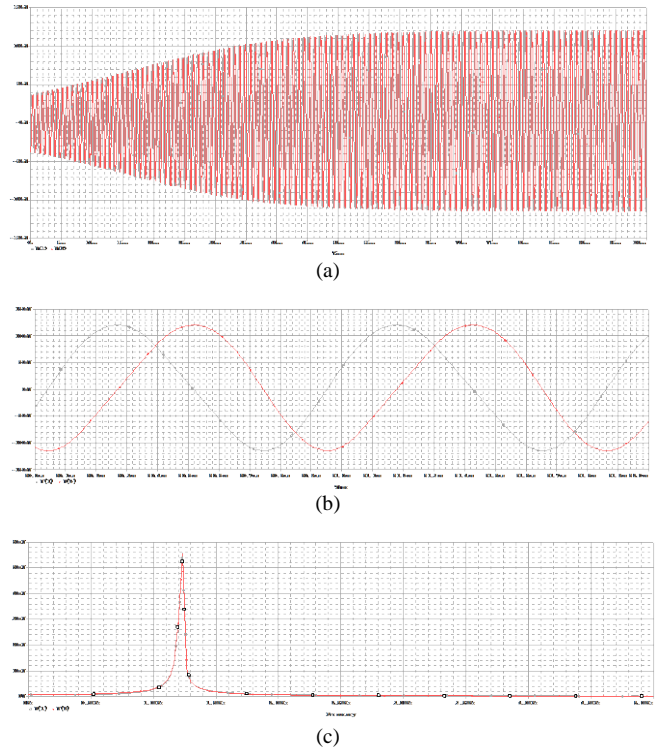

(a)

(b)

(c)

Fig. 6 Simulation results of the quadrature sinusoidal oscillator circuit by using CMOS based CCCII. (a) Initial state waveform (b) Steady state waveform (c) The frequency spectrum

B. AD844 Based CCCII Simulation Results

Another simulation is done by using the AD844 SPICE Macro-model parameters to check the workability of the presented circuit. The circuit is supplied with symmetrical ±10 V and the passive component values taken in simulation are as shown Table I. As it is done before, two simulations are done for the circuits employing CCII and CCCII. The oscillation frequency and THD values obtained from the simulations are given in Table IV.

TABLE IV. OSCILLATION FREQUENCY AND THD VALUES FOR AD844 IMPLEMENTATION

	Circuit employing CCII		Circuit employing CCCII	
Oscillation Frequency (MHz)	1.20		1.23	
THD %	V(1)	V(2)	V(1)	V(2)
	4.6	4.3	1.6	3.4

Also in AD844 based CCCII implementation, the THD values of the circuit are better than the values of the circuit employing CCII as shown in Table IV. The power dissipation of the circuit employing CCCII is 659 mW for the initial voltage of 0.1 mV given to C_1. The quadrature phase error is 0.64 %.

The voltage waveforms of the proposed circuit employing AD844 based CCCII are shown in Fig.7.
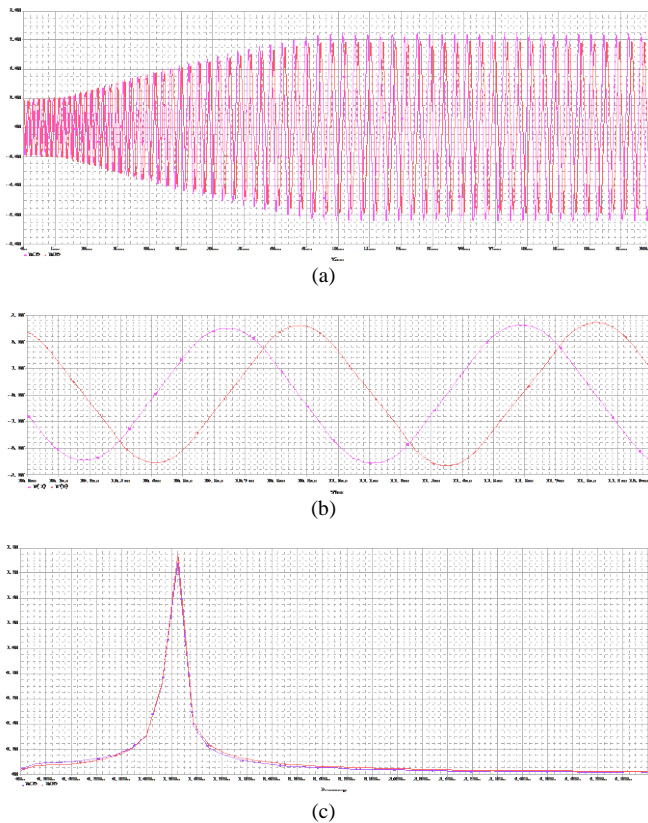
(a)

(b)

(c)

Fig. 7 Simulation results of the quadrature sinusoidal oscillator circuit by using AD844 based CCCII. (a) Initial state waveform (b) Steady state waveform (c) The frequency spectrum

VI. CONCLUSION

A voltage-mode MOS-C quadrature sinusoidal oscillator based on CCCII has been presented. The resistors used in the circuit are implemented by MOS transistors and the capacitors are all grounded. So, the proposed circuit is fully integrable and it is possible to adjust the oscillation frequency by external MOS gate voltage. The simulation results agree well with the theoretical analysis. The proposed circuit achieves a good THD performance and the quadrature phase error is quite low. It is stated that the CCCII employing circuits enhance the circuit performance significantly when compared to the same topology employing CCII. The workability of the presented circuit is also verified by using commercially available AD844. It is expected that the proposed circuit will be useful in various telecommunication and signal processing applications.

ACKNOWLEDGMENT

REFERENCES

[1] R. Senani, D. R. Bhaskar, "Single op-amp sinusoidal oscillators suitable for generation of very low frequencies," *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 4, 1991, pp. 777–779.

[2] R. Holzel, "Simple wide-band sine wave quadrature oscillator," *IEEE Transactions on Instrumentation and Measurement*, vol. 42, no. 3, 1993, pp. 758–760.

[3] I. A. Khan, S. Khwaja, "An integrable gm-C quadrature oscillator", *International Journal of Electronics*, vol. 87, 2000, pp. 1353-1357.

[4] D. R. Bhaskar, R. Senani, "New CFOA-based single-element-controlled sinusoidal oscillators," IEEE Transactions on Instrumentation and Measurement, vol. 55, no. 6, 2006, pp. 2014–2021.

[5] J. W. Horng, C. L.Hou, C.M. Chang, W.-Y. Chung, H.-W. Tang, Y-H.Wen, "Quadrature oscillators using CCIIs', *International Journal of Electronics*, vol. 92, 2005, pp. 21–31.

[6] S. S. Gupta, R. Senani, "Grounded capacitor SRCOs using differential difference complementary current feedback amplifier," *IEEE Proc. Circuits Devices Syst* , vol. 152, 2005, pp38-48.

[7] M. T. Ahmed, I. A. Khan, N. Minhaj, "On transconductance-C quadrature oscillators," *International Journal of Electronics*, vol. 83, 1997, pp. 201-207.

[8] J. Mohan, S. Maheshwari, I. A. Khan, "Mixed mode quadrature oscillator using a single FDCCII," *Journal of Active Passive Electron. Devices*, vol.2, 2007, pp. 227–234.

[9] M. T. Abuelma'atti, H. A. Alzaher, "Comment on current mode quadrature sinusoidal oscillator using single FTFN," *International Journal of Electronics*, vol. 85, 1998, pp. 177-180.

[10] S. S. Gupta, R. Senani, "Realization of current mode SRCOs using all grounded passive elements'", Frequenz, 57, 2003, pp. 26–37.

[11] W. Tangsrirat, S. Pisitchalermpong, "CDBA-based quadrature sinusoidal oscillator," Frequenz, , vol. 61, 2007, pp. 102-104.

[12] A. U. Keskin, C. Aydin, E. Hanciolu, C. Acar, "Quadrature oscillator using current differencing buffered amplifiers (CDBA)," Frequenz, vol. 60, 2006, pp. 21-23.

[13] A. U. Keskin, D. Biolek, "Current mode quadrature oscillator using current differencing transconductance amplifiers (CDTA)," *IEE Proc.-Circuits, Devices and Systems*, vol. 153, 2006, pp. 214-218.

[14] D. Biolek, V. Biolkova, A. U. Keskin, "Current mode quadrature oscillator using two CDTAs and two grounded capacitors", In Proceedings of the 5th WSEAS Int. Conf. on System Science and Simulation in Engineering, Tenerife, Canary Islands (Spain), December 16-18, 2006, pp. 368-370.

[15] S. Pisitchalermpong, D. Prasertsom, T. Piyatat, W. Tangsrirat, W. Surakampontorn, "Current Tunable Quadrature Oscillator Using Only CCCDBAs and Grounded Capacitors", The 2007 ECTI International Conference, 4th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, Thailand, May 9-12, 2007, pp. 32-35.

[16] N. Minhaj, "Dual-Output Second-Generation Current Conveyor-based Voltage-Mode Sinusoidal Oscillator modified for Chaos Generators", *International Journal of Recent Trends in Engineering*, Vol 2, no. 5, 2009, pp. 315-318.

[17] A. Lahiri, "Low Frequency quadrature sinusoidal oscillators using current differencing buffered amplifiers", *Indian Journal of Pure&Applied Physics*, vol. 49, 2011, pp. 423-428.

[18] P. Gupta, P. Kumar Jain, D. S. Ajnar, R. Kumar sahu, "Design of sinusoidal oscillator using second generation current conveyor", Paripex Indian Journal of Research, Vol.2, Issue: 3, 2013, pp. 129-131.

[19] A. M. Soliman, "Current-mode oscillators using single output current conveyors", *Microelectronics Journal*, vol. 29, 1998, pp. 907-912.

[20] R. Keawon, W.Jaikla, "A Resistor-less Current-mode Quadrature Sinusoidal Oscillator Employing Single CCCDTA and Grounded Capacitors", Przeglad Electrotechniczny (Electrical Review), ISSN 0033-2097, R. 87 NR 8/2011, pp. 138-141.

[21] G. Sharma, J. Kaur, N. Gupta, "Current Conveyor Based Sinusoidal Oscillator with its Application", *International Journal of Science and Research (IJSR)*, vol. 3 Issue 5, 2014, pp. 1897-1900.

[22] K. Koli, "CMOS Current Amplifiers: Speed versus Nonlinearity", Phd Thesis, Department of Electrical and Communications Engineering, Helsinki University of Technology, Espoo, Finland, November, 2000.

[23] A. Gökçen, "New Possibilities in The Design of Analog Integrated Circuit with MOS-C Realization", Phd Thesis, Graduate School of Natural and Applied Sciences, Dokuz Eylül University, İzmir, Turkey, June, 2010.

[24] S. N. Songkla, W. Jaikla, "Realization of Electronically Tunable Current-mode First-order Allpass Filter and Its Application", *International Conference on Electrical, Computer, Electronics and Communication Engineering*, Italy, 28-29 February 2012, pp. 40-43.