

FPGA based Omnidirectional Video Acquisition Device (OVAD)

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Abstract Nowadays, together with development of technology, and thus utilization of unmanned systems such as UAVs, providing wide field of view constantly becomes more and more important. One of solutions designed to solve that problem is OVAD (Omnidirectional Video Acquisition Device). A device, which was implemented using analog cameras and STM32 microcontroller, has proven its validity during testing process. The device may be found as useful in many applications, both civilian and military. However, size and weight of the device made it difficult to implement OVAD on small unmanned vehicles. Proposed solution is FPGA based OVAD, which is result of OVAD further development.

Keywords—omnidirectional camera, image processing, FPGA.

I. INTRODUCTION

The problem of omnidirectional video acquisition is an issue, which has been considered for many years, by engineers throughout the world. The need for providing 360 degrees of horizontal or vertical field of view is present among many branches of contemporary industry, such as surveillance systems, military, robotics, etc. In example, cameras, providing half-spherical field of view are widely used in military applications such as unmanned vehicles, where a necessity of observing all of vehicle surroundings is inevitable. Moreover, most of the time, success of a mission depends on information provided by vision system.

Nowadays, there are many devices, which can be a solution of the problem of omnidirectional video acquisition. One of them is a camera equipped with fisheye lens (Fig. 1, section c). Utilization of this particular type of lens creates a possibility to acquire video from a very wide angle. One of its greatest advantages is that this device does not include moving parts, which is associated with low susceptibility to external factors, such as shocks or adverse weather conditions. However, the image acquired by the device is significantly distorted [1]. Lens distortion, the fifth of the Seidel aberrations, is manifested by distortion of acquired image, which depends on the distance from its optical centre [2]. The occurrence of distortion always results in corruption of information carried by the image, while software elimination of distortion is always connected to loss of the information.

This work has been supported by Applied Research Programme of the National Centre for Research and Development as a project ID 178438 path A - Costume for acquisition of human movement based on IMU sensors with collection, visualization and data analysis software

Another, often utilized solution is PTZ camera (pan-tilt-zoom camera) (Fig. 1, section a). This device is based on utilization of one or more servomotors, which rotate the camera. Such a solution may prove imperfect in situations, when moving parts are exposed to dusty or pollinated environment. In this environment moving parts may become blocked, which may result in permanent damage of servomotor. If that situation occurs, the camera loses all of its original functionality, allowing only one direction of video acquisition [1].

The device, which combines advantages and eliminates disadvantages of both PTZ cameras and devices utilizing fisheye lenses is OVAD (Omnidirectional Video Acquisition Device) [1], presented in Fig. 1, section b. OVAD is made of multiple cameras, which are positioned statically in a way that provides 360 degrees of horizontal field of view. Video streams, acquired by adjacent cameras are combined into panorama. Thanks to that solution OVAD provides 360 degree of horizontal field of view without utilization of any moving elements, while preventing image from being significantly distorted. It is possible to immediately change the direction of video acquisition. Furthermore, failure of one cameras results only in losing part of field of view, while it does not cause a total loss of information, as in solutions based on single camera. Unfortunately, this solution has one major disadvantage. It is caused by utilization of analog cameras, which are too large and heavy to be able to be used on small vehicles, such as UAV (Unmanned Aerial Vehicle) [18-20].

Solution to the problems mentioned is utilization of digital cameras, which may have significantly smaller dimensions than analog cameras, while preserving similar quality of acquired video stream. However, the solution requires a system capable of real-time collecting and processing data acquired from multiple cameras. That problem is solved by utilization of FPGA, which are capable of parallel processing.

Utilization of FPGA in vision processing is not a new concept. Among present implementations, known are many solutions, such as using FPGA to process video data acquired from thermal [11], hyperspectral [12] and conventional cameras [16]. Another example of using FPGA in modern concepts is implementation of image processing algorithms, low-level, operating individual pixels, intermediate-level, converting pixels to a different representations (e.g. histogram, DFT, etc.), as well as high-level algorithms, designed to extract meaning from an image, [13, 17, 21] such as optical

flow extraction [15] or analysis of an image using neural networks, basing on FPGA allowance to access a number of subroutines in parallel [12].

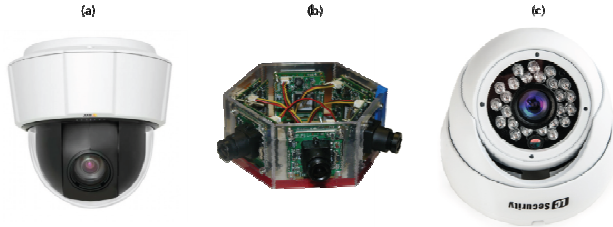


Fig. 1 PTZ camera AXIS P5532-E (a), OVAD (b), LC-1120 FISHEYE Premium (c) [1].

II. HARDWARE

Selection of appropriate equipment used to create FPGA based OVAD is very important task. Utilized parts have to be capable of real-time video acquisition, which involves collecting and processing data acquired from multiple cameras. Implementation of hardware required selection of cameras, FPGA and RAM used to store one frame obtained by each camera.

A. Cameras

Utilized cameras are OmniVision OVM7690 (Fig. 2). Maximum resolution of video acquired by that devices is 640x480. Their biggest advantage is small size and weight. Selected parameters of the cameras are presented in Table 1 [8].



Fig. 2 OVM7690 camera [10].

Before starting an acquisition every camera has to be properly configured. Configuration of OmniVision devices is being carried through SCCB (Serial Camera Control Bus), 2-wire interface similar to I²C. 2-wire SCCB consists of two master-slave connections: SCL and SDA. SCL line is used to transmit clock signal, while SDA is a bidirectional data line. Each subsequent byte is transmitted in 9 clock cycles. During the first 8 cycles data byte is transmitted, from MSB to LSB. The last, 9th cycle is used to determine whether information sent was acknowledged by destined device. During that cycle, when receiver acknowledges received byte, it forces low state on SDA line [3]. Operation of writing value to camera register requires sending three consecutive bytes. The first one contains 7-bit word containing slave device ID and one bit which carries information whether an incoming operation will be write register value or read register value. Second byte, called sub-address byte, contains 8-bit address of chosen

register, to which configuration data (sent in third telegram) is supposed to be written.

Parameter	Value
Active array size	640 x 480
operating temp. range	-30°C to 70°C
stable image temp. range	0°C to 50°C
output formats	YUV422 / YCbCr422, RGB565, CCIR656, raw RGB
input clock frequency	6 ~ 27 MHz
maximum image transfer rate	VGA (640x480): 30 FPS QVGA (320x240): 60FPS
package dimensions	2517μm x 2967μm x 2465μm

Table 1. Cameras specifications given by manufacturer.

B. Field-programmable Gate Array (FPGA)

Acquisition of data from multiple cameras means, that, in every second, huge amount of data will flow through the system. Maintaining real-time processing of the data means, that the device must be based on either CPU with relatively high computing abilities or CPU capable of parallel processing, when the same performance can be achieved at much lower clock frequencies. Parallel processing can be achieved through utilization of FPGA, which, along with pipelining is intrinsic resource of FPGA.

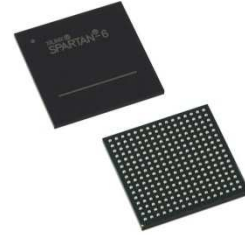


Fig. 3 Xilinx Spartan-6 XC6SLX16 [10].

FPGAs are composed of an array of independent components, called CLB (Configurable Logic Block). These elements can perform complex or simple logic functions such as logic gates, multiplexers, flip-flops, etc. They are connected to each other via configurable bus network, managed by interconnect blocks. Thanks to that feature, it is possible to configure FPGA in a way that two or more independent tasks can be executed in parallel to each other.

Configurable logic blocks are configured through filling LUT (Look-up table), a table, where all ready-made solutions, for every possible combination of inputs, are stored. Utilization of LUTs makes complex logical functions extremely simplified, every calculation can be performed in one clock cycle. Moreover, execution of parallel, independent components implemented in FPGA, does not require to be synchronized with a single clock signal [14]. Components can be triggered from any input, which means that FPGAs are capable of asynchronous processing.

Field-programmable Gate Array used in the device is Xilinx Spartan-6 XC6SLX16 [4] (Fig. 3.), available on Digilent

Nexys™ 3 Spartan-6 FPGA Board [9]. The board is equipped with 100MHz oscillator, however, according to datasheet [9], via utilization of DCM (Digital Clock Manager) and PLL (Phase-Locked Loop), clocking frequency can be increased to a value greater than 500MHz. FPGA based OVAD does not use that feature, because memory used in that device can be clocked at maximum frequency of 80MHz [7].

C. Memory

Maintaining independence between displaying and collecting of data acquired by multiple cameras requires storing a single frame from each camera. FPGAs, despite their incredible computing capability, proves very inefficient in terms of storing large amount of data. Every modern FPGA is backed up by dedicated memory blocks, called BlockRAM. However, BlockRAM capacity is not sufficient to store one frame obtained even by single camera. In consequence, use of external memory was necessary.

Used FPGA is placed on Digilent Nexys™ 3 Spartan-6 FPGA Board (Fig. 5.). The same board includes three components designed for memory storage: 16Mbyte Micron Cellular RAM, 16Mbyte Micron Parallel PCM and 16Mbyte Micron Quad-mode SPI PCM [9]. From the perspective of FPGA based OVAD, the best solution turned out to be Micron MT45W8MW16 [7] (Fig. 4.), which has 16bit parallel data bus and 23bit address bus. When working at maximum possible clock frequency equal to 80MHz, chosen memory can perform operation of write and read fast enough to store data acquired from several cameras. The memory can operate in two modes – asynchronous and burst. The most convenient option would be using asynchronous mode, however, in that mode, required time interval between two data operations is 100ns, which means maximum clocking speed equal to 10MHz. This maximum frequency is insufficient for real-time data acquisition. Therefore, it was necessary to use burst mode. Disadvantages of the mode are delay associated with the initialization of read or write operation, and inability of interspersing of read and write operations during single burst. However, after proper read/write burst initialization, memory can store up to 128 16bit words at a frequency of up to 80MHz (in a single burst), which is advantageous from the point of view of the described problem.

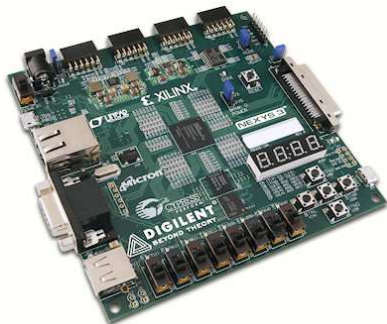


Fig. 4 Digilent Nexys 3 Spartan-6 FPGA Board [9].

III. IMPLEMENTATION

FPGA program has been written in VHDL language. Due to compatibility of the selected FPGA with the software provided by manufacturer, used development tool is Xilinx ISE Design Suite 14.7.

One of assumptions made during implementation planning was full application modularity. Required elements (defined in VHDL as components), which had to be implemented on FPGA are: component which handles data acquisition from camera, component which configures all cameras, component responsible for handling memory, and component responsible for handling the output. The output of FPGA based OVAD is a D-Sub connector, via which video is transmitted to receiver. Video standard used by the device is VGA (Video Graphics Array). Main advantage of modular approach is that parts, such as cameras or memory, can be easily replaced with different types. Exchange would mean updating or replacing of only single component, but should not affect the rest of program implemented on FPGA.

The implemented solution uses asynchronous processing, supported by FPGA, due to the need of connecting components triggered by clock signals running at different frequencies. Each camera transmits its own, independent PCLK (Pixel CLock) signal, indicating, that pixel is ready to receive, while external memory works at frequency of 80 MHz. Subsequent components of camera-memory-display path are connected via asynchronous FIFO (First In First Out) buffers. This solution supports memory working in burst mode, when during single burst write and read operations cannot intersperse. By utilization of FIFO buffers, pixels ready to be written into memory are not lost when read operation is performed, but are stored in adequate buffers. FIFO buffers have been generated by IP Core Generator, and provide asynchronous work at frequency of read/write operation up to 500MHz [5]. IP Core Generator is an integral part of Xilinx ISE Design Suite and was also used to generate component providing all necessary clock signals (prescaler) [6].

Schematic, which describes the program implemented in FPGA is shown in Fig.6. The first step is to configure cameras via SCCB interface. At the same time memory configuration is performed. When configuration of all cameras ends, component responsible of configuration of cameras sets *acq_en* output, which triggers start of video acquisition. Data acquired by each camera is stored in adequate FIFO buffer. When FIFO buffer, used to store incoming data, is half-full, a signal is sent to memory management module, which stores write requests in its own operation queue. After executing all previous requests, write burst operation is performed. A similar situation occurs during processing data acquired to the display control module. When FIFO, used to store output data, is half-empty, request to read more data from memory is sent to memory management module, and stored in operation queue. Therefore, when memory is working at frequency, that provides appropriate read and write speed, FIFO used to store incoming pixels will never overflow, and FIFO used to store output data will never become empty.

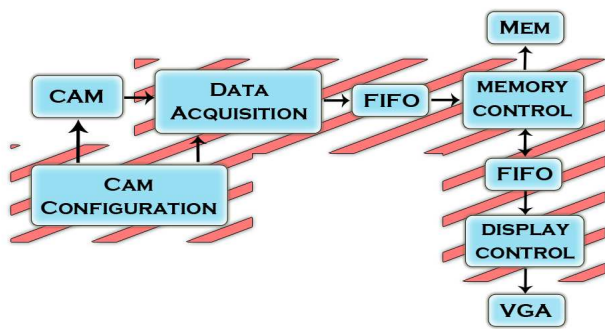


Fig. 5 Simplified schematic presenting interconnections between modules. Modules marked with red stripes are implemented using FPGA.

IV. SUMMARY

Use The implemented solution has proven to be the right approach in further development of OVAD. In the age of digital technology, utilization of digital cameras, backed up by FPGA and external memory, resulted in significant improvement in comparison with the previous version of the device. Main advantages, which should be distinguished, are:

- reducing size of device, while maintaining quality of acquired image – use of cameras, which dimensions are $2517\mu\text{m} \times 2967\mu\text{m} \times 2465\mu\text{m}$ resulted in significant reduction of size and weight of the device,
- ease of processing and analysis of digital image – transfer of an digital image is less vulnerable to transmission disturbances; moreover, flexibility in choosing transmission interface is evident. It is possible to use widely-used interfaces, such as Ethernet, USB, etc.,
- extended prospects for further development – utilization of respectively advanced FPGA creates a possibility to use cameras able to acquire higher resolution video, moreover, creates a flexibility of choosing the way of presenting and storing of data acquired, as well as possibility to implement additional modules designed for analysis and processing the acquired data, without changing the physical structure of the device.

In conclusion, similarly to OVAD, FPGA based OVAD can be found useful in many branches of technology, both civilian and military. Resistance to weather condition (in comparison to PTZ camera), as well as insignificant optical distortion (in comparison to camera equipped with fisheye lens), makes the device competitive option among existing solutions. In addition, costs of the device may still be several times less than the price of PTZ cameras.

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