MODELING of dislocation evolution in Multi-junction based Photovoltaic devices

Tarek M. Hatem and Mohamed T. Elewa

***Abstract*—**Genuine Processing techniques have been developed to minimize density of dislocations and other defects originating from thermal stresses present in Multi Junction PVs. Embedded Void Approach; (EVA) was used to address the defects evolution in GaAs growth on Si substrates. In attempts to study void effect on dislocation generation; elastic models were prepared for voided and un-voided structures. Stresses and displacements were compared and related to alteration in dislocation density.

***Keywords*—**Dislocation Density, Multi-junction solar cells, Finite Element Modeling, Thermal Stresses

I. Introduction

THE achievement of a PV device that collects photons in 1.4 eV-1.0 eV range requires considerable effort. It happens to be the main obstacle in achieving cascade solar cells with conversion $\eta > 45\%$. In attempts to address this dilemma, N was added to GaAs forming GaAsN to reduce Eg to ~1.0 eV while maintaining the lattice matched conditions to GaAs. The result was poor diffusion length, minority carrier lifetime, and low open circuit voltage [1]. Following the early reports, where an inverted structure of InGaP grown on GaAs substrate, lattice constant is graded to grow $In_{0.3}Ga_{0.7}As$ followed by etching off the GaAs substrate, the problem is in handling ultra-thin film in large scale production [2]. InGaAs/GaAsP strained layered super-lattice (SLS) was lattice matched to GaAs and was reported successful to partially absorb photons in the 1.4 – 1.2 eV range however it required hundreds of SLS periods to fully absorb 1.4 – 1.0 eV, [3]. GaAs growth on Si substrates seem to offer the solution for the 1.0 eV sub cell problem, unfortunately GaAs/Si experiences thermal expansion mismatch of 54%, and a lattice mismatch of 4.1% These mismatches initiate dislocations at the interface that run through the crystalline structure of the films and terminate at free surfaces. Dislocations act as scattering centers affecting carriers' lifetime and setting a limit on the performance, reliability, and lifetime of MJ-PV devices. Voids act as a free surface for inhibiting dislocation propagation, this was the main principle of Embedded Void Approach (EVA) [4] where a high density of micro-voids—a few micrometers in length and less than a micrometer in diameter—are introduced into the GaAs layer near its interface with Si. Experimentally, the three dimensional void network has an average density of about 10^8 cm^{-2}, dislocations could be reduced uniformly over large area of substrates, by two orders of magnitude from 10^9 cm^{-2} to 10^7 cm^{-2}, [5]. Dislocations propagate to voids in their vicinity or can be redirected to be trapped in the three dimensional networks. Voids act as expansion joints for lattice mismatches as well. In this paper, the problem is parsed numerically where defects evolution is simulated during the processing of GaAs/Si device whileaccounting for temperature variations. A static study was performed on two elastic models, to confirm effect of void on defect density.

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II. Procedure

*V*oid generation process is a three-step process that involves growth, etching and regrowth. It begins with growth of GaAs on a Si substrate by Metal-Organic Chemical Vapor Deposition (MOCVD) at temperatures greater than 600°C, this initiates intrinsic stresses, followed by annealing at elevated temperature around 1000°C for stress relaxation. GaAs is then etched, using mask-less inductively coupled plasma- reactive ion etching mask-less (ICP-RIE), to expose different planes of GaAs and generate Nanowires (NWs). These planes have different growth rates of GaAs facets, thus generating voids filled with low-pressure gas H_2. In the final step, epitaxial GaAs is overgrown on the GaAs NW template and again followed by annealing for stress relaxation.

Numerically, an Elastic continuum Model was built, GaAs/Si device was modeled with dimensions 30 μmx 12.5 μm for width and length, respectively. The Sketch chiefly focused at the interface region where a partition divided the length into two non-equal parts; GaAs has length of 2.5 μm wh*ereas* Si length is 10 μm, voids have random size and vertical orientation with average length of 1 micro*meter*. Material Properties identified for Si and GaAs are listed in table 1. Simulation was run on ABAQUS software. Unit system used was MPA, as classified by ANSYS, which is similar to SI and CGS unit systems, where mass is in tones; length is in mm and pressure in MPa. Young's Modulus and Poisson's Ratio for both materials were considered for (111) plane; closely packed plane. Material Parameters selected are listed in table *I*in appendix. Static general analysis was performed where maximum number of increments was 1, minimum increment size of $1e^{-5}$ and maximum of 1.

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Thermal stresses occur when structure temperature drops from 1000°C, annealing temperature to 25°C, room temperature. The model experiences two steps each with the assigned temperature. Displacement Constraints were applied by using boundary conditions to the top right node of the substrate in x and y, since all translational and rotational degrees of freedom need to be constrained, i.e. U1= U2= UR3=0. For inspecting the validity of stress reduction with voids, the previous procedure was carried out for Void and no-Void models. Approximate mesh global seed size of 0.0005. The un-voided model was structure-meshed; voids were free meshed with minimized mesh transition medial axis as complex geometry prevailed. For both models, Element shape was Quadratic and Element type was set to CPS4R, denoting 4-node bilinear, plane stress, quadrilateral, reduced integration. The finite element mesh contained 2171 nodes and 1994 elements for mesh with voids wh*ereas* un-voided mesh contained 1586 nodes and 1500 elements. Results based on average element output at nodes, averaging threshold 75%

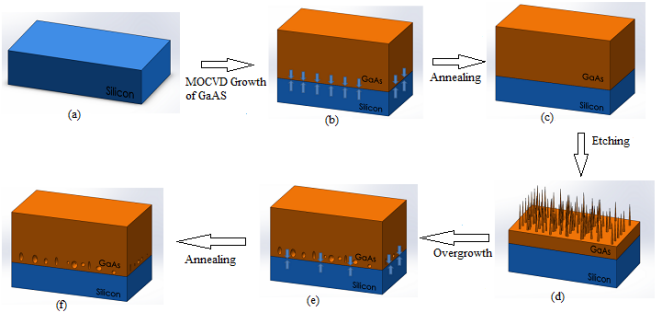

Figure1EVA Fabrication process chart a) Silicon Substrate b) MOCVD growth c) Annealing d) Etching e) Overgrowth and creating voids f) Annealing

III. Discussion

After implementing nearly 20 voids in the voided structure, it should be mentioned that obtained interface stress results, measured from silicon substrate, were reduced from *216 MPa*, without voids to *186 MPa* with voids. Whereas stresses measured from GaAs are *265 MPa*with voids and*216 MPa*without. Stress value at top of GaAs film was higher for voided structure; stresses peaked at the center of film top with*186 MPa*, without voids stress value is *173 MPa***.** An explanation for raise in stress is that voids act as discontinuities or stress singularities in the structure levitating stresses while annihilating dislocations. It is the main purpose of EVA to reduce defects number which act as barriers for charge carriers in the semiconductors; voids result in higher fatigue and less defects. Lower surface stresses signify less dislocation densities. Stress Contour plots acquired are shown in fig. 1 and 2 for both models. Substrate bottom stresses were reduced significantly from *108 MPa* to *79.5 MPa* when voids were applied. Maximum Spatial Displacement, *0.141 μm***,** occurred at top of film left side**,** for voided model. Same BCs were applied to un-voided model; the displacement had a higher value of *0.158 μm*. Spatial displacement plots are shown in fig. 3 and 4. It was perceived that voids closer to the interface, yielded higher stress values, at that region, than those at a greater distance from the interface. Unfortunately, when voids are shifted upwards, they raise stresses at other regions i.e. GaAs film top. Void network positioning is crucial. Moreover, it was noticed that resulting stresses depend on void density; this was confirmed when a stress of *248 MPa* at GaAs and *124 MPa* at Si layer were obtained after implementing 40 voids.

Assuming an elastic response from, the effect of raising temperature from T_0 to T initiates thermal stress, σ_T which is given by

$$\Delta\sigma_T = E\,\Delta\alpha\,\Delta T \quad (1)$$

Where $\Delta\alpha$is difference in thermal expansion coefficient in K^{-1} between substrate and film ($\Delta\alpha=\alpha_s-\alpha_f$), ΔT is change in temperature, E is Youngs Modulus. For Silicon thermal stress is *431 MPa* and *814.3 MPa* for GaAs. Since the two materials are considered isotropic ($\varepsilon=\varepsilon_x=\varepsilon_y$, $\sigma=\sigma_x=\sigma_y$), the misfit stress in the upper layer is

$$\sigma^T = \frac{-E_i(\alpha_i-\alpha_s)}{(1-\nu_i)} * \left(T - T_0^i\right) + \sigma_i^I \quad (2)$$

Where i denotes layer number, normally this is the stress present in upper layer when the substrate is ultimately thick compared to film thickness, $h_s/h_f<<<1$. The equations for top film stress σ and average film stress $\bar{\sigma}$ are related to film/substrate thickness ratio ($\xi=h_f/h_s$) and Biaxial Young's Modulus ratio$\Sigma = \frac{E_2/(1-\nu_2)}{E_1/(1-\nu_1)}$as seen in (Hutchinson [1996]). Equations for top film stress σ and average film stress$\bar{\sigma}$are given by the following relations [6]

$$\frac{\bar{\sigma}}{\sigma^T} = \frac{1+\Sigma\xi^3}{(\Sigma\xi^2-1)^2+4\Sigma\xi(\xi+1)^2} \quad (3)$$

$$\frac{\sigma}{\sigma^T} = \frac{1-3\Sigma\xi^2-2\Sigma\xi^3}{(\Sigma\xi^2-1)^2+4\Sigma\xi(\xi+1)^2} \quad (4)$$

The curvature of the bilayer could be concluded as

$$\kappa = \frac{1+\xi}{1+\Sigma\xi^3} * \frac{6(1-\nu_1)h_2\bar{\sigma}}{E_1h_1^2} \quad (5)$$

The curvature of the bilayer could also be calculated. Radius of curvature ρ=1/κ, where κ is in mm. Mismatch stress in GaAs layer is *653.9 MPa* with a negative sign indicating compression, while stress at film top is *226 MPa*, higher by *50 MPa* than that obtained from simulation, and average film stress is *286.6 MPa*. Curvature Value is 232 corresponding to a curvature radius of *4.32 mm*. Applying basic Pythagoras Theorem on nodal displacement on model without voids, curvature of radius was found to be *5.24 mm*. While a radius of *7.03 mm* was obtained for voided model. Curvature radius indicates the variation of the unit tangent direction, the higher the curvature radius, the less the deflection.

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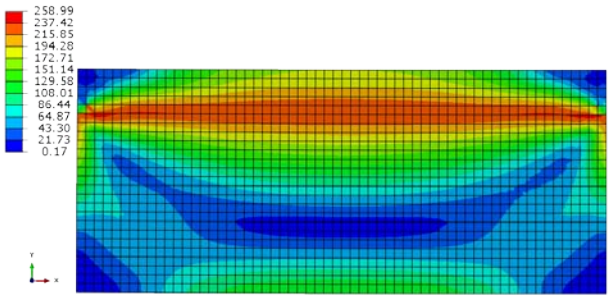

Figure2Von Mises Stress Average 75% without voids

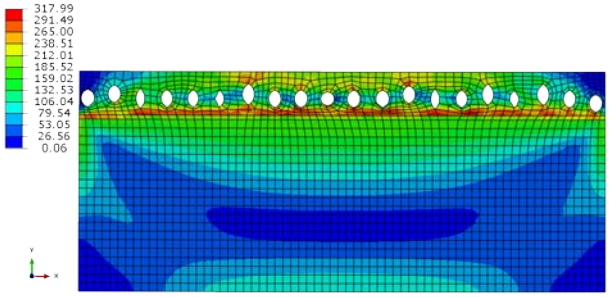

Figure3Von Mises Stress with Voids

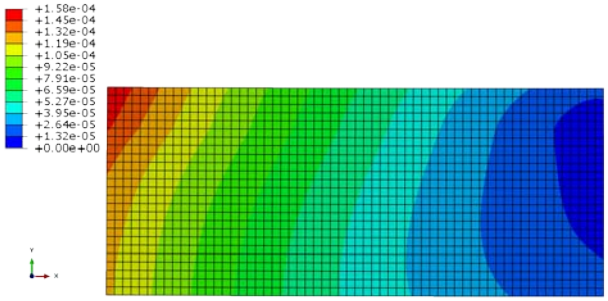

Figure4 Spatial Displacement without Voids

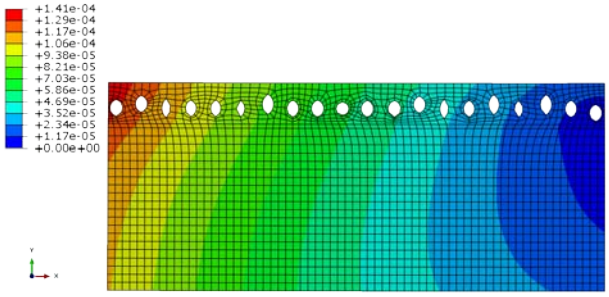

Figure5Spatial Displacement with Voids

IV. Conclusion

In conclusion, thermal stresses and therefore dislocations have shown reduction when voids where introduced near the interface of GaAs/Si cell. The paper discussed two elastic models illustrating void effect on dislocation density. A reduction in stress at Si layer of 14% while GaAs stresses rose to 18%, reduction in maximum displacement is 11%. The approach may address a solution for the 1.0 eV sub cell problem; permitting an efficiency raise to 45%. Void density and positioning should be controlled for stress reduction.

Appendix

Table I

Parameter	Si	GaAs	Unit
Young's Modulus	168.9	144	GPa
Poisson's Ratio	0.262	0.31	—
Density	$2.33e^{-9}$	$5.32e^{-9}$	ton/mm^3
CTE (α)	$2.616\ e^{-6}$	$5.8\ e^{-6}$	K^{-1}
Slip System	{111} $<\bar{1}10>$	{111} <110>	—
Lattice Constant	0.543106	0.56533	nm

Acknowledgment

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